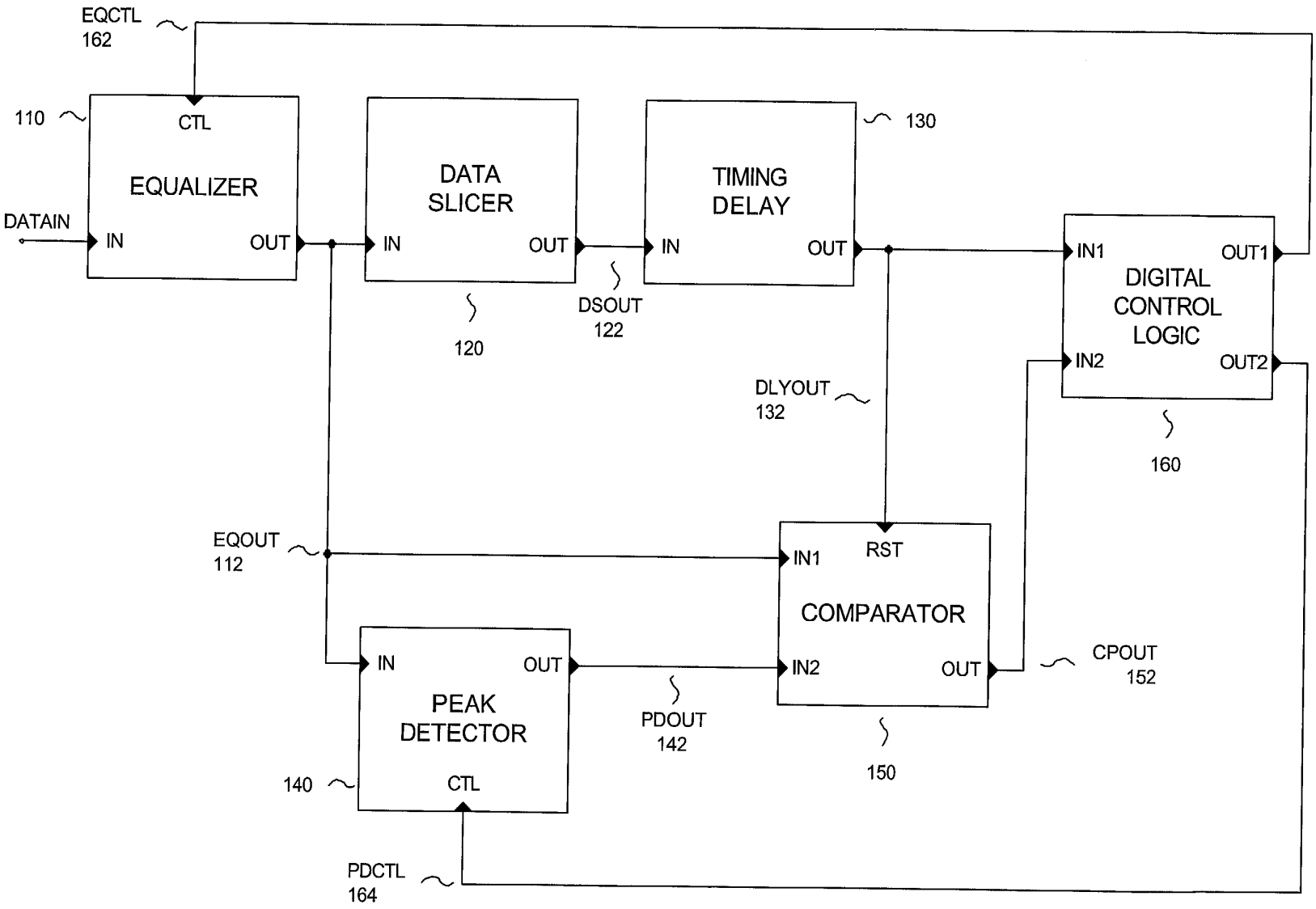
EQCTL
162
110
CTL
EQUALIZER
DATAIN
IN
OUT
DATA
SLICER
IN
OUT
120
DSOUT
122
TIMING
DELAY
130
IN
OUT
DIGITAL
CONTROL
LOGIC
IN1
OUT1
IN2
OUT2
160
DLYOUT
132
EQOUT
112
IN1
RST
COMPARATOR
IN2
OUT
CPOUT
152
150
IN
OUT
PEAK
DETECTOR
CTL
140
PDOUT
142
PDCTL
164

FIGURE 1

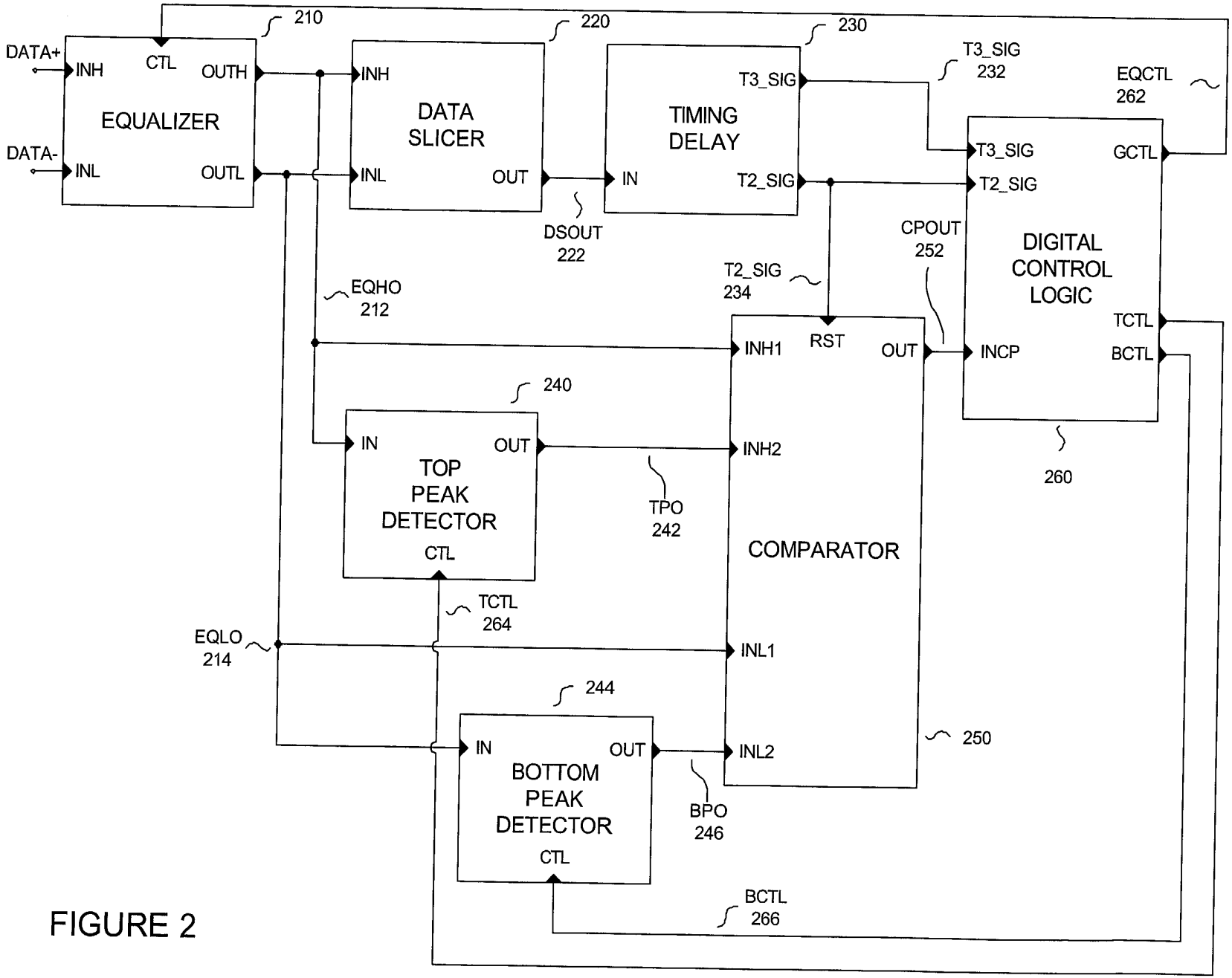
DATA+
DATA-
INH
INL
CTL
OUTH
OUTL
EQUALIZER
210
INH
INL
OUT
DATA SLICER
220
DSOUT
222
IN
T2_SIG
T3_SIG
TIMING DELAY
230
T3_SIG
232
EQCTL
262
T3_SIG
T2_SIG
GCTL
DIGITAL CONTROL LOGIC
TCTL
BCTL
INCP
CPOUT
252
260
EQHO
212
T2_SIG
234
RST
INH1
OUT
240
IN
OUT
TOP PEAK DETECTOR
CTL
INH2
TPO
242
COMPARATOR
TCTL
264
EQLO
214
INL1
244
IN
OUT
BOTTOM PEAK DETECTOR
CTL
INL2
250
BPO
246
BCTL
266

FIGURE 2

PATENT APPLICATION

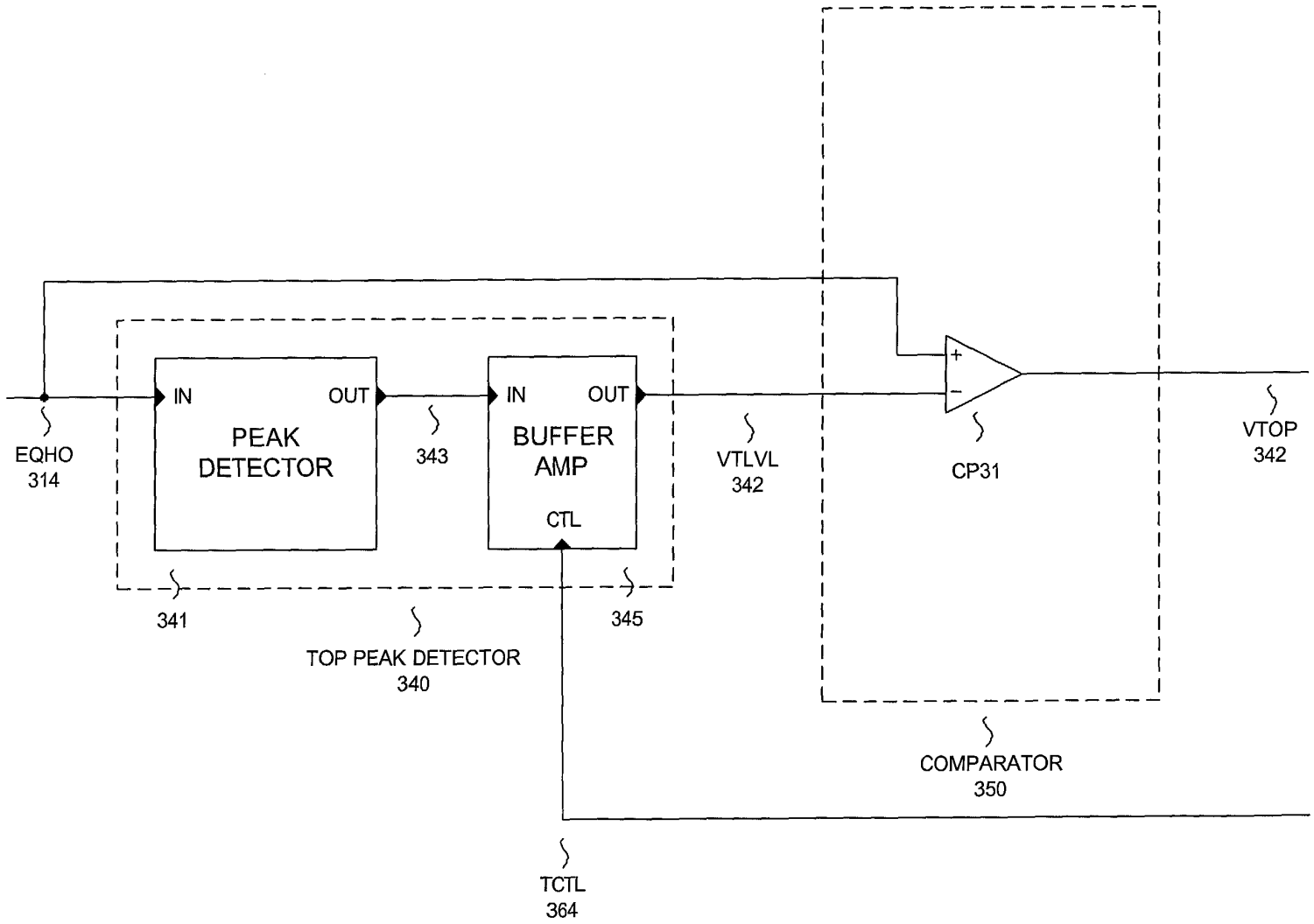

FIGURE 3

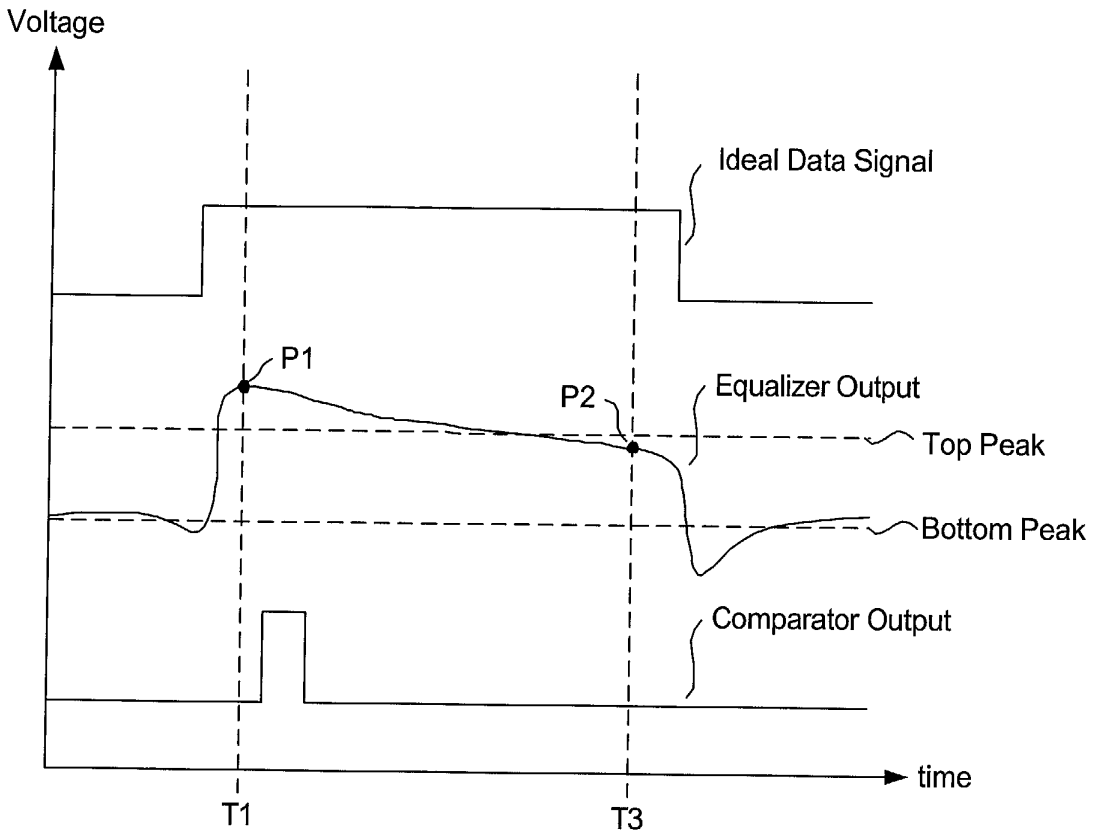
Voltage
Ideal Data Signal
P1
P2
Equalizer Output
Top Peak
Bottom Peak
Comparator Output
time
T1
T3

FIGURE 4

Patent Application

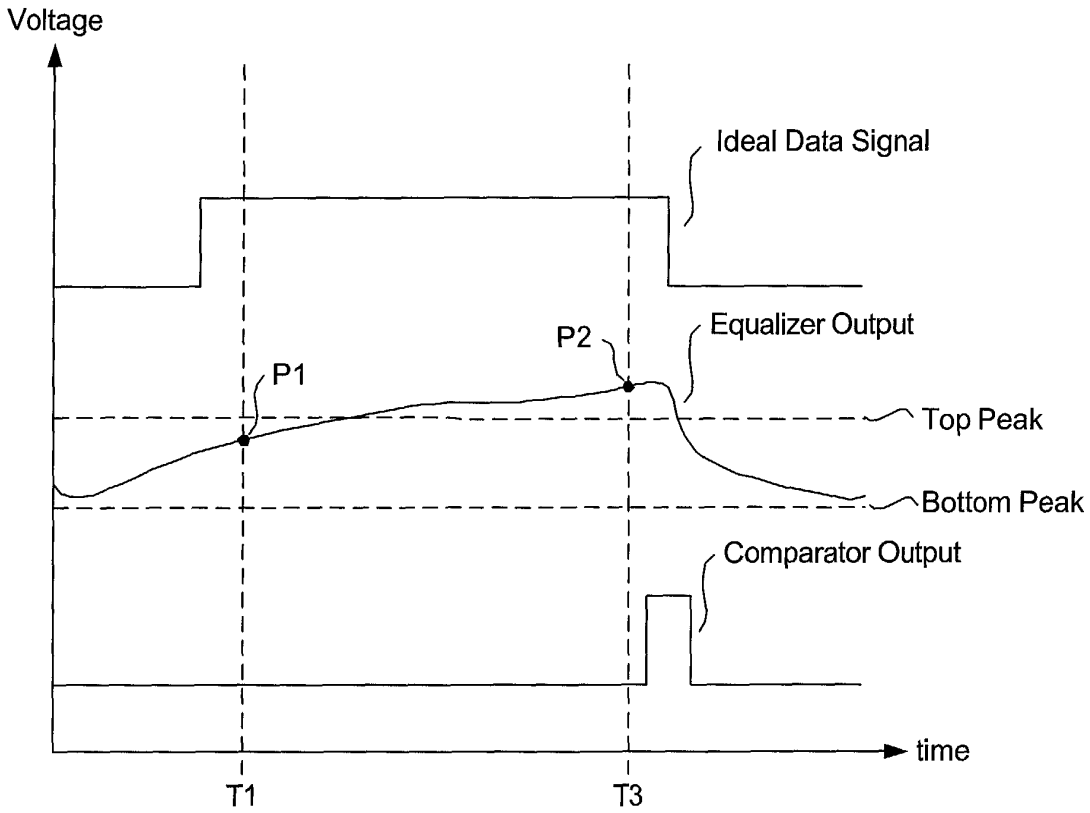

FIGURE 5

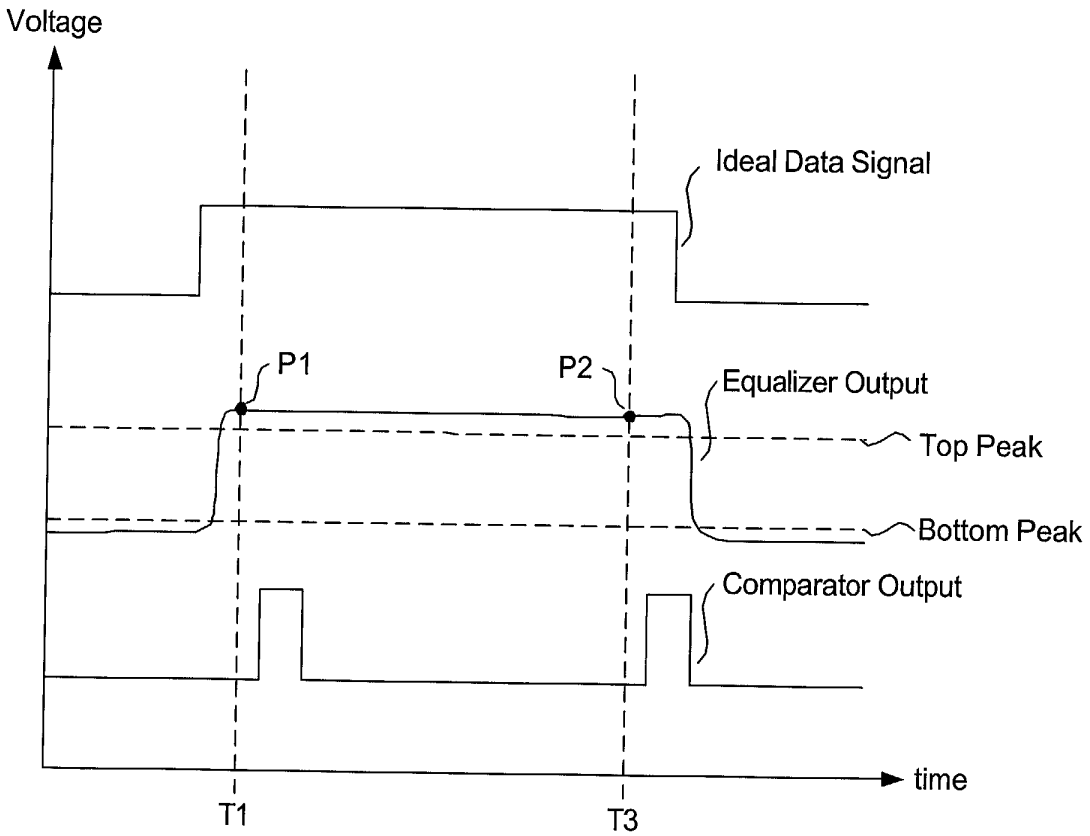
Voltage
Ideal Data Signal
P1
P2
Equalizer Output
Top Peak
Bottom Peak
Comparator Output
time
T1
T3

FIGURE 6

Tobacco Seeds

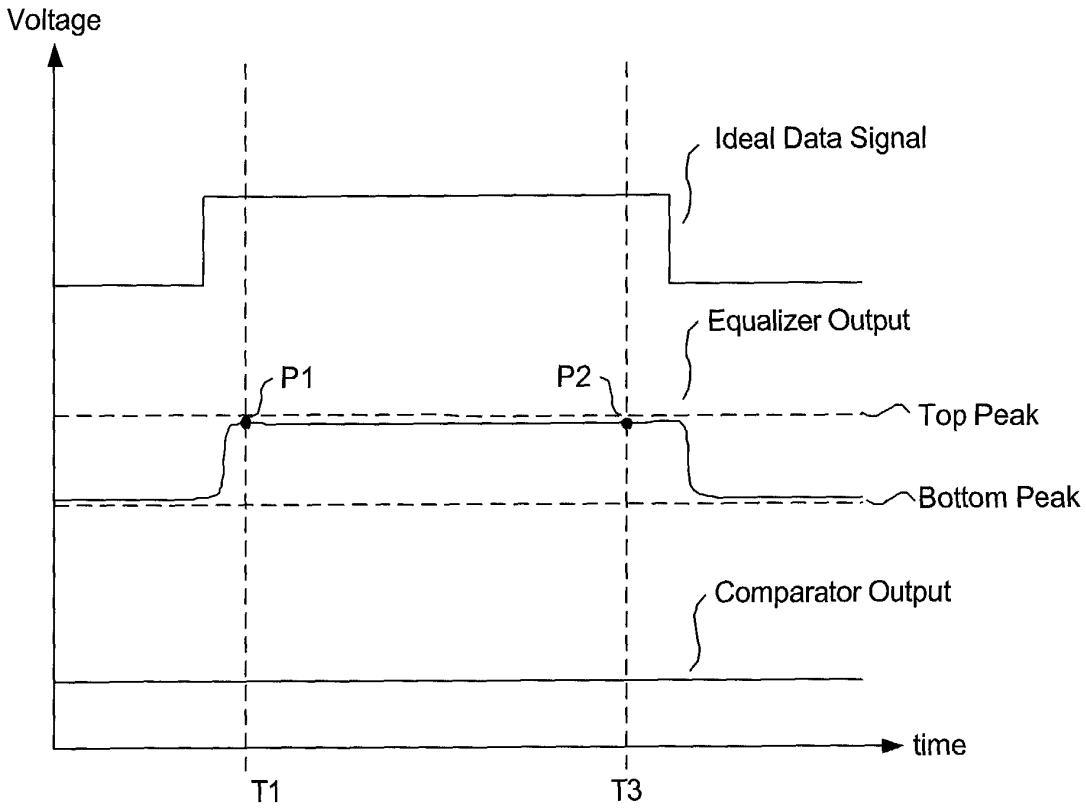

FIGURE 7

PATENT APPLICATION

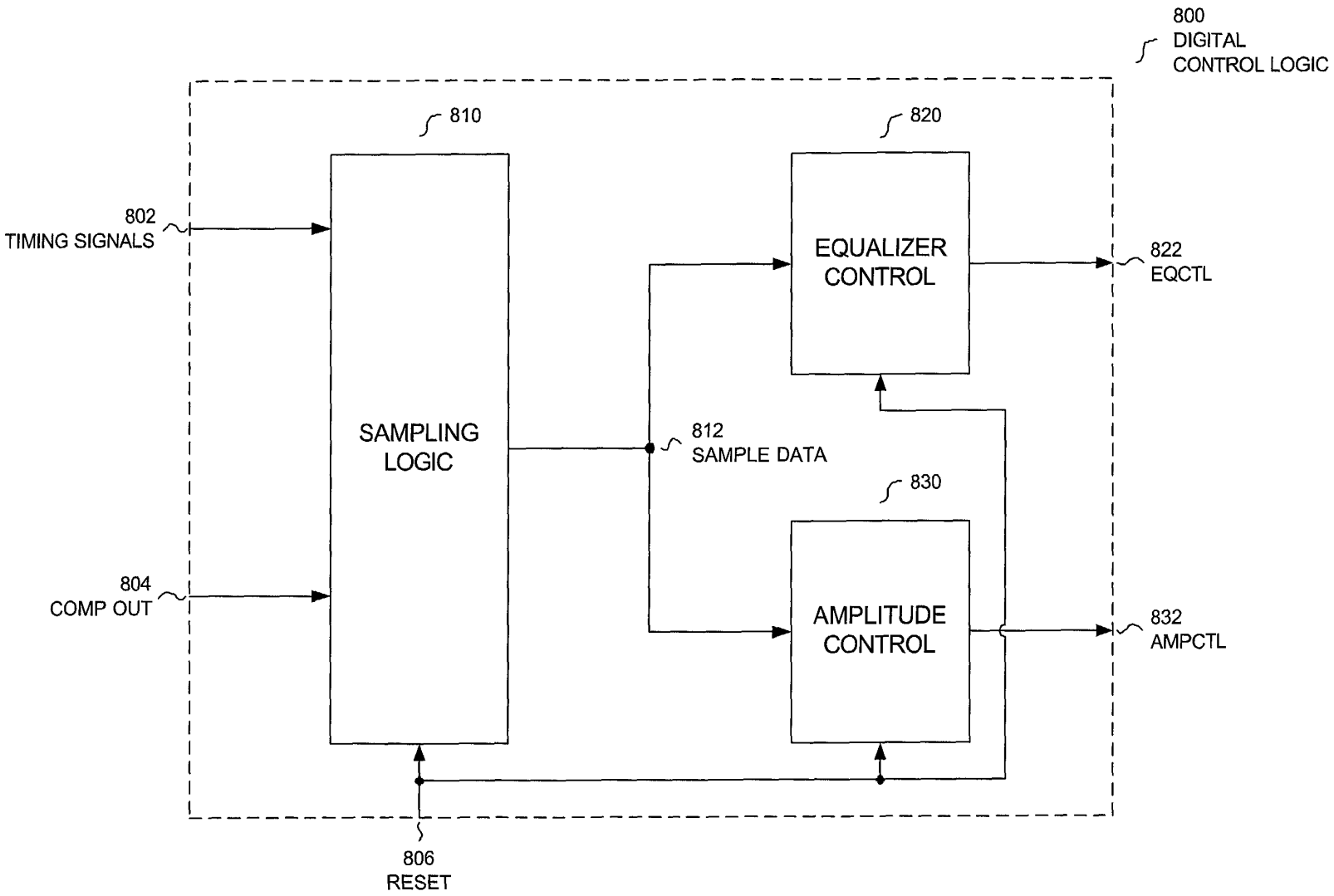

FIGURE 8

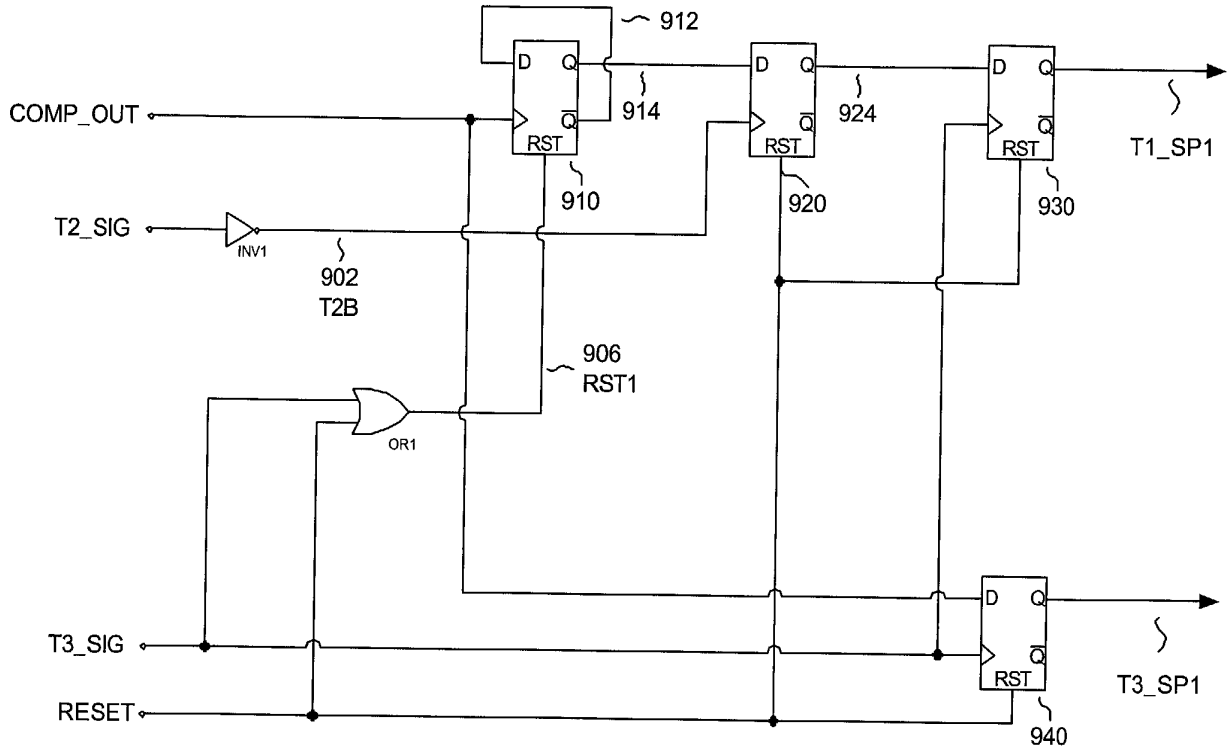
912
D
Q
RST
914
924
930
T1_SP1
COMP_OUT
T2_SIG
INV1
902
T2B
910
920
906
RST1
OR1
T3_SIG
RESET
T3_SP1
940

FIGURE 9

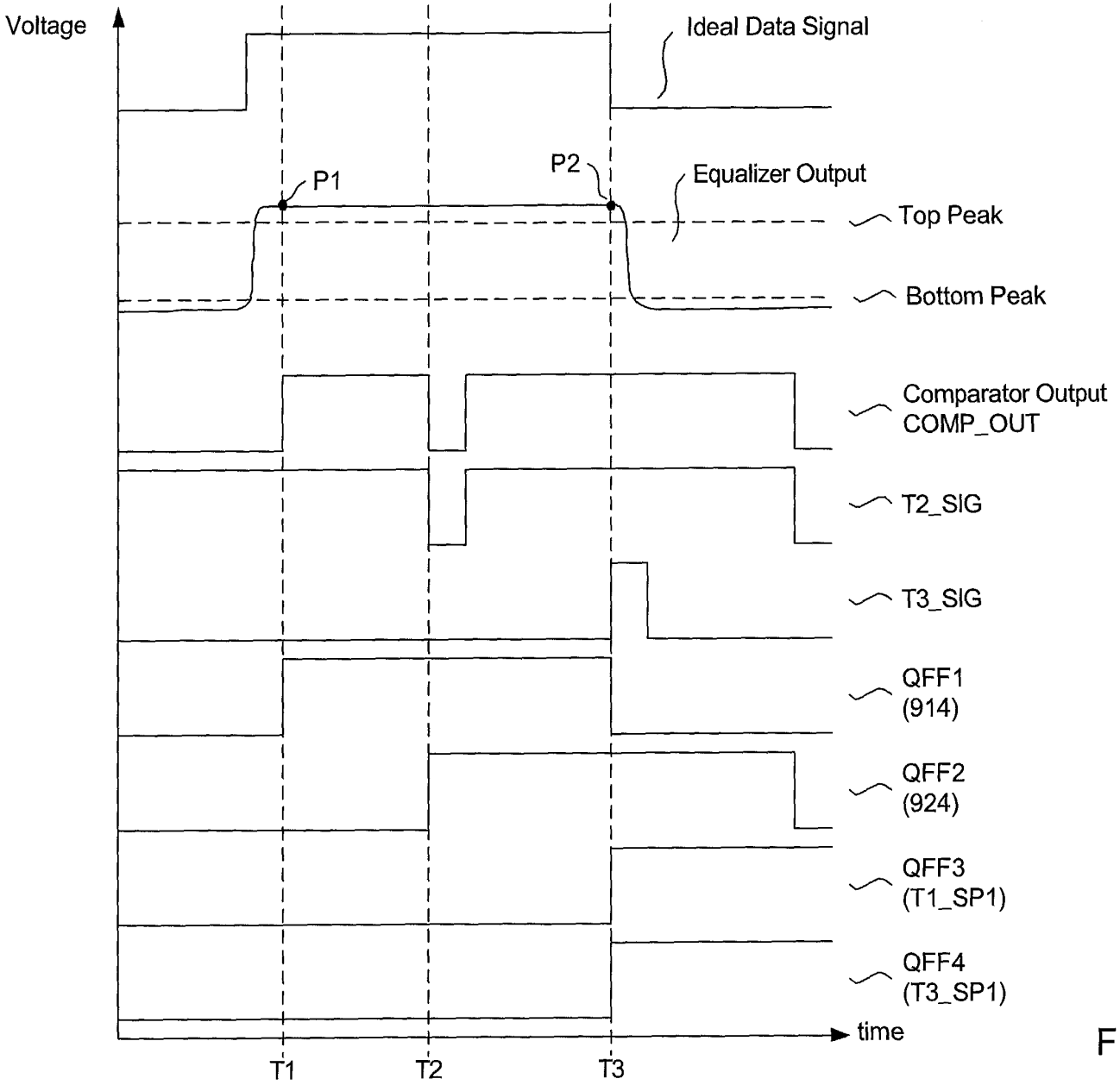
Voltage
Ideal Data Signal
P1
P2
Equalizer Output
Top Peak
Bottom Peak
Comparator Output
COMP_OUT
T2_SIG
T3_SIG
QFF1
(914)
QFF2
(924)
QFF3
(T1_SP1)
QFF4
(T3_SP1)
time
T1
T2
T3

FIGURE 10

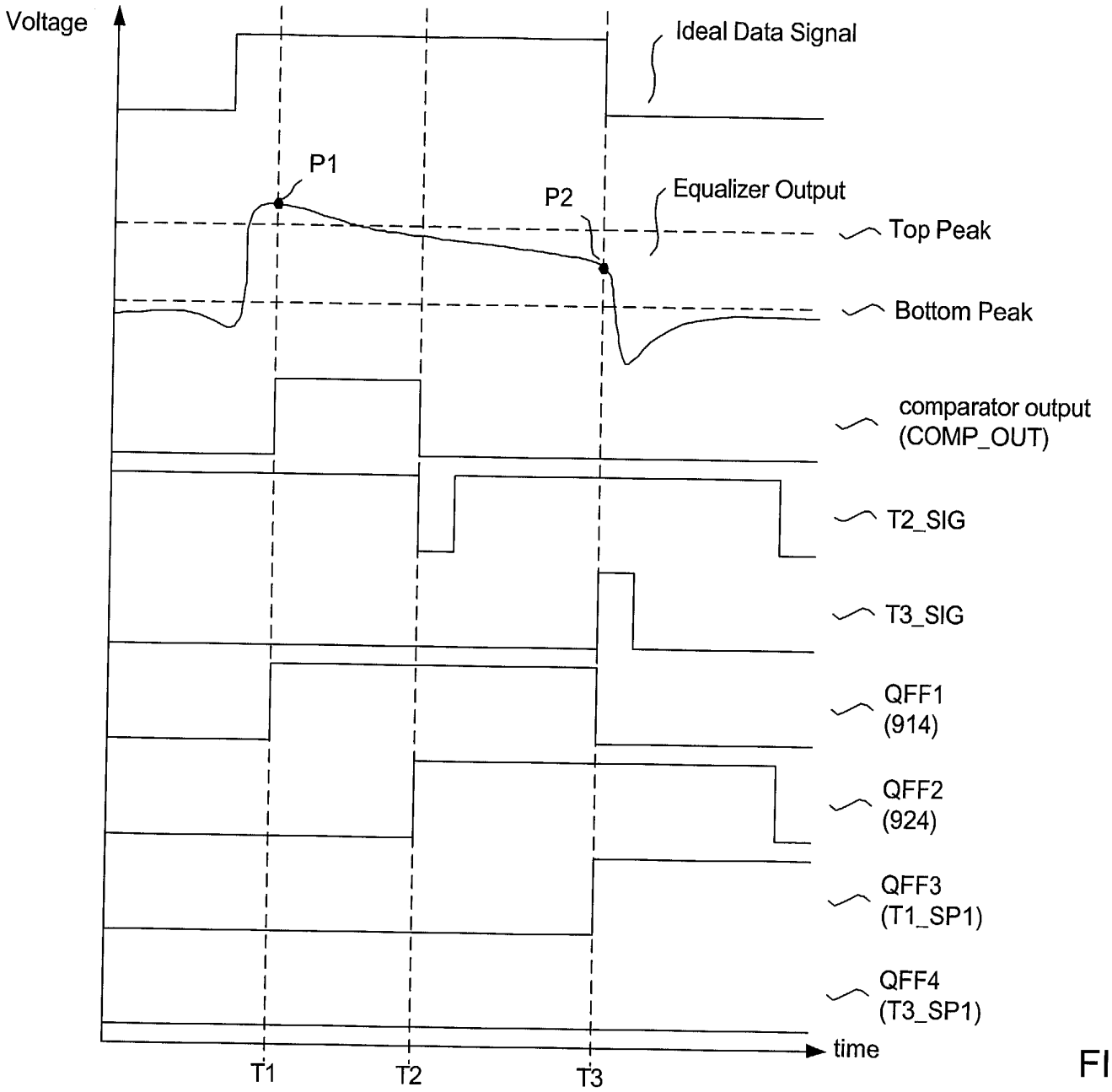
Voltage
Ideal Data Signal
P1
P2
Equalizer Output
Top Peak
Bottom Peak
comparator output
(COMP_OUT)
T2_SIG
T3_SIG
QFF1
(914)
QFF2
(924)
QFF3
(T1_SP1)
QFF4
(T3_SP1)
time
T1
T2
T3

FIGURE 11

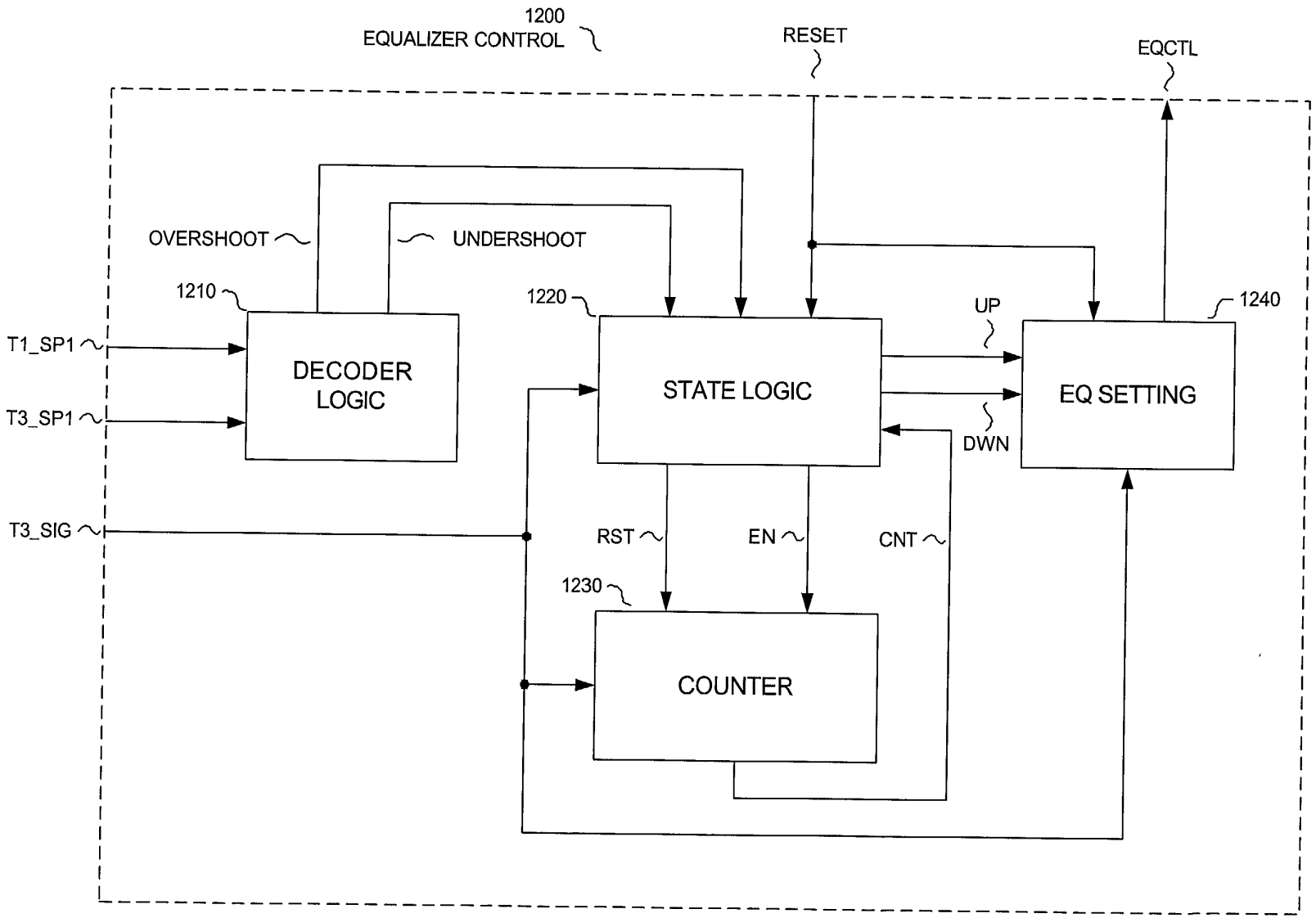
1200
EQUALIZER CONTROL
RESET
EQCTL
OVERSHOOT
UNDERSHOOT
1210
1220
UP
1240
T1_SP1
T3_SP1
DECODER LOGIC
STATE LOGIC
EQ SETTING
DWN
T3_SIG
RST
EN
CNT
1230
COUNTER

FIGURE 12

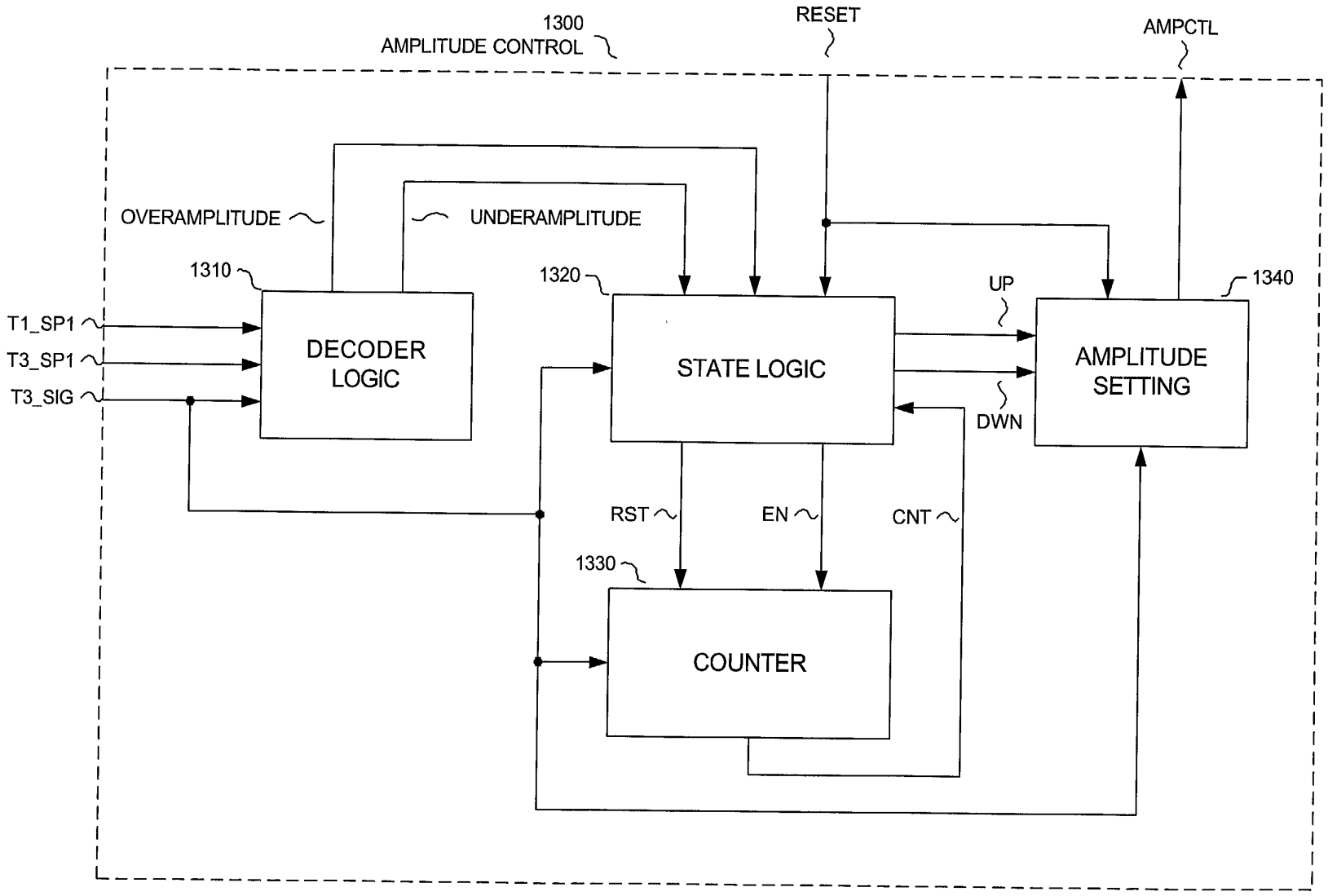
1300
AMPLITUDE CONTROL
RESET
AMPCTL
OVERAMPLITUDE
UNDERAMPLITUDE
1310
1320
1340
T1_SP1
T3_SP1
T3_SIG
DECODER LOGIC
STATE LOGIC
AMPLITUDE SETTING
UP
DWN
RST
EN
CNT
1330
COUNTER

FIGURE 13